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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/782,513	02/18/2004	Alexander Burinskiy	08211/0200373-US0/P05759	4709

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/782,513	BURINSKIY ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,12,16 and 17* is/are rejected.

7)☒ Claim(s) *9-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim objection

Claims 7 and 17, the phase "sense resistor" should be --sense transistor--.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 and 6-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Ichiki (JP 2001-185964).

As to claim 1, Ichiki discloses in figure 3B a current regulation circuit, comprising: a current mirror (201, 202p) arranged with a sense transistor (201p) and a power transistor (202p); a current sink that is coupled to a drain of the sense transistor (as shown), wherein the current sink pulls down a drain voltage of the sense resistor if a current flowing through the power transistor is less than a limit; and a control component (the comparator) that is arranged to limit the current flowing through the power transistor if the drain voltage of the sense resistor is substantially equivalent to a drain voltage of the power transistor.

As to claim 6, figure 3B shows that the control component senses a feedback signal provided by a load coupled to a drain of the power amplifier, wherein the feedback signal is employed in the control of the operation of the control component.

As to claim 7, figure 4 shows that the current mirror of the power transistor and the sense resistor employs a ratio of m:1.

As to claim 8, figure 4 shows that the sense transistor and the power transistor are at least field effect transistors (FET).

3. Claims 1-8, 12, 16 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Magoon (USP 6744795).

As to claim 1, Magoon discloses in figure 4 a current regulation circuit (302, 305, 306, 312, 326). It is noted that column 4, lines 61-65, teaches that the transistors may be p-channel FETs. Therefore, the connections and polarities of elements in circuit 300 are reversed, such as shown in Shuzo's figure 3B cited above. Magoon's current regulation circuit comprising: a current mirror (p channel FETs 305 and 306) arranged with a sense transistor (305) and a power transistor (306); a current sink (302) that is coupled to a drain of the sense transistor, wherein the current sink pulls down a drain voltage of the sense resistor if a current flowing through the power transistor is less than a limit; and a control component (326) that is arranged to limit the current flowing through the power transistor if the drain voltage of the sense resistor is substantially equivalent to a drain voltage of the power transistor.

As to claim 2, figure 4 further shows a component (312) that outputs a signal if the drain voltage of the sense resistor is substantially equivalent to the drain voltage of the power transistor.

As to claim 3, figure 4 shows that the component (312) is at least one of a comparator and a differential amplifier.

As to claim 4, figure 4 shows that the control component employs the signal to substantially turn off the current flowing through the power transistor.

As to claim 5, figure 4 shows that the control component employs the signal to modulate the amount of current flowing through the power transistor to be less than the limit.

As to claim 6, figure 4 shows that the control component senses a feedback signal provided by a load coupled to a drain of the power amplifier, wherein the feedback signal is employed in the control of the operation of the control component.

As to claim 7, figure 4 shows that the current mirror of the power transistor and the sense resistor employs a ratio of m:1.

As to claim 8, figure 4 shows that the sense transistor and the power transistor are at least field effect transistors (FET).

As to claim 12, figure 4 shows a current regulator, comprising a current mirror (p channel FETs 305 and 306) arranged with a sense transistor (305) and a power transistor (306), a current sink (302) that is coupled to a drain of the sense transistor, wherein the current sink pulls down a drain voltage of the sense resistor if a current flowing through the power transistor is less than a limit; a control component (326) that is arranged to limit the current flowing through the power transistor if the drain voltage of the sense resistor is substantially equivalent to a drain voltage of the power transistor; and a comparison component (312) that presents a signal if the drain voltage of the sense resistor is substantially equivalent to the drain voltage of the power transistor.

As to claim 16, figure 4 shows that the current flowing through the power transistor is substantially continuous.

As to claim 17, figure 4 shows a current regulation circuit, comprising a means (connection line) for mirroring current flowing in a sense transistor (305) and a power transistor (306), a means (302) for sinking current that is coupled to a drain of the sense transistor, wherein the current sink pulls down a drain voltage of the sense resistor if a current flowing through the power transistor is less than a limit; a means (326) for limiting the current flowing through the power transistor if the drain voltage of the sense transistor is substantially equivalent to a drain voltage of the power transistor; and a means (312) for presenting a signal if the drain voltage of the sense transistor is substantially equivalent to the drain voltage of the power transistor.

Allowable Subject Matter

4. Claims 9-11 and 13-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 9-11 and 13 would be allowable because the prior art fails to teach or suggest a clock signal that enables the regulation of a switching current flowing through the power transistor.

Claims 14 and 15 would be allowable because the prior art fails to teach or suggest a first switch and a second switch for operating with a switching current flowing through the power transistor, wherein the first switch enables an output of the control component to be coupled to at least the power transistor and the sense transistor and wherein the second switch enables signal presented by the comparison component to be coupled to the control component, and wherein the comparison component's signal indicates if the drain voltage of the sense resistor is substantially equivalent to a drain voltage of the power transistor.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

April 7, 2005